IN THE CLAIMS:

1. (Canceled)

2. (Currently Amended) A ~~The~~ nonvolatile semiconductor memory device ~~as claimed in claim 1,~~ comprising:

a plurality of blocks each having a nonvolatile memory cell array; and

a program potential generating circuit which supplies a program potential to the nonvolatile memory cell array,

wherein said program potential generating circuit adjusts the program potential according to a first address signal selecting one of said blocks and a second address signal indicating a position of a write-accessed memory cell in said one of said blocks, and

wherein said program potential generating circuit includes:

a booster circuit which generates a boosted potential; and

a regulator circuit which generates the program potential according to the boosted potential and a reference potential, wherein the program potential generated by said regulator circuit is adjusted according to the first address signal and the second address signal.

3. (Original) The nonvolatile semiconductor memory device as claimed in claim 2, wherein said regulator circuit includes:

a capacitance circuit which generates a comparison potential by dividing the program potential by use of capacitances;

a differential amplifier circuit which generates the program potential from the boosted potential in response to a comparison between the comparison potential and the reference potential; and

a circuit which adjusts the capacitances of said capacitance circuit according to the first address signal and the second address signal.

4. (Canceled)

5. (Currently Amended) A ~~The~~ nonvolatile semiconductor memory device ~~as claimed in claim 4,~~ comprising:

a plurality of blocks each having a nonvolatile memory cell array;

a program potential generating circuit which supplies a program potential to the nonvolatile memory cell array, wherein said program potential generating circuit adjusts the program potential according to a first address signal selecting one of said blocks and a second address signal indicating a position of a write-accessed memory cell in said one of said blocks; and

a program potential adjusting circuit which generates a program potential adjusting signal according to the first address signal and the second address signal,

wherein said program potential generating circuit adjusts the program potential according to the program potential adjusting signal, and

wherein said program potential adjusting circuit performs inversion control that either inverts or does not invert the second address signal, depending on the first address signal, and supplies the second address signal having undergone the inversion

control to said program potential generating circuit as the program potential adjusting signal.

6. (Currently Amended) A ~~The~~ nonvolatile semiconductor memory device ~~as claimed in claim 1,~~ comprising:

a plurality of blocks each having a nonvolatile memory cell array; and

a program potential generating circuit which supplies a program potential to the nonvolatile memory cell array,

wherein said program potential generating circuit adjusts the program potential according to a first address signal selecting one of said blocks and a second address signal indicating a position of a write-accessed memory cell in said one of said blocks, and

wherein two of said blocks have different arrangements of a second address represented by the second address signal such that the second address is arranged in reversed orders between the two blocks in relation to distance from said program potential generating circuit, the program potential being adjusted according to the second address signal after identifying one of the two blocks according to the first address signal, such as to reflect a physical distance from said program potential generating circuit to the position of the write-accessed memory cell.

7. (Canceled)

8. (New) The nonvolatile semiconductor memory device as claimed in claim 5, wherein said plurality of blocks each includes a redundancy memory cell, and said program potential adjusting circuit generates the program potential adjusting signal independently of the second address signal if said redundancy memory cell is selected, the program potential adjusting signal reflecting an actual wire length from said program potential generating circuit to the selected redundancy memory cell.